In the claims:

Claims 1 to 8 (canceled)

Claim 9 (withdrawn) A transistor which comprises:

(a) a semiconductor substrate having a surface and having a first source/drain region and a second source/drain region spaced apart from each other and extending to said surface; and

(b) a channel region disposed in said substrate between said first and second source/drain regions in said substrate and extending to said surface, said channel region having a first dopant profile contacting said first source/drain region to provide a first V_T and a second dopant profile different from said first dopant profile contacting said second source/drain region to provide a second V_T different from said first V_T.

Claim 10 (currently amended) A transistor which comprises:

(a) a semiconductor substrate having first and second spaced apart source/drain ~~and drain~~ regions therein; and

(b) a channel region between said source/drain ~~and drain~~ regions in said substrate having a relatively low V_T central region between said source/drain ~~and drain~~ regions and relatively high V_T regions adjacent to said source/drain ~~and drain~~ regions,~~; wherein~~ said channel region ~~is~~ having an implanted ~~low~~ one of a positive or negative V_T dopant intermediate said source/drain ~~and drain~~ regions and having an implanted ~~high~~ one of a negative or positive V_T dopant adjacent said source/drain ~~and drain~~ regions, the opposite of said dopant in said channel region.

Claim 11 (withdrawn) The transistor of claim 9 wherein said first dopant profile is a relatively low V_T dopant implant and said second dopant profile is a selective relatively high V_T dopant implant.